Intel® E7205 Chipset Memory Controller Hub (MCH)

Specification Update

December 2002

Notice: The Intel® E7205 chipset MCH may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are documented in this Specification Update.

Document Number: 251938-002

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Contents

Revision History 4
Preface 5
Errata 9
Specification Changes 11
Specification Clarifications 13
Documentation Changes 15

Revision History

Revision	Description	Date
-001	Initial Release	November 2002
-002	Updated Errata E1 & E2.	December 2002

Preface

This document is an update to the specifications contained in the documents listed in the following Affected Documents/Related Documents table. It is a compilation of device and document errata and specification clarifications and changes, and is intended for hardware system manufacturers and for software developers of applications, operating system, and tools.

Information types defined in the Nomenclature section of this document are consolidated into this update document and are no longer published in other documents. This document may also contain information that has not been previously published.

Affected Documents/Related Documents

Document Title	Document Number
Intel® E7205 Chipset Memory Controller Hub (MCH) Datasheet	251937-001

Nomenclature

Specification Changes are modifications to the current published specifications. These changes will be incorporated in the next release of the specifications.

Errata are design defects or errors. Errata may cause the behavior of the Intel® E7205 chipset MCH to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present on all devices.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in the next release of the specifications.

Documentation Changes include typos, errors, or omissions from the current published specifications. These changes will be incorporated in the next release of the specifications.

Component Identification via Programming Interface

The Intel® E7205 chipset MCH stepping can be identified by the following register contents:

Stepping	Vendor ID[1]	Device ID[2]	Revision Number[3]
B0	8086h	255Dh	03h

NOTES:
1. The Vendor ID corresponds to bits 15:0 of the Vendor ID Register located at offset 00–01h in the PCI function 0 configuration space.
2. The Device ID corresponds to bits 15:0 of the Device ID Register located at offset 02–03h in the PCI function 0 configuration space.
3. The Revision Number corresponds to bits 7:0 of the Revision ID Register located at offset 08h in the PCI function 0 configuration space.

Component Marking Information

The Intel® E7205 chipset MCH may be identified by the following component markings:

Stepping	S-Spec	Top Marking	Notes
B0	SL65P	RGE7205MC	

Summary Tables of Changes

The following table indicates the Specification Changes, Errata, Specification Clarifications or Documentation Changes, which apply to the listed Intel® E7205 chipset MCH steppings. Intel intends to fix some of the errata in a future stepping of the component, and to account for the other outstanding issues through documentation or Specification Changes as noted. This table uses the following notations:

Codes Used in Summary Table

X:	Erratum, Specification Change or Clarification that applies to this stepping.
Doc:	Document change or update that will be implemented.
PlanFix:	This erratum may be fixed in a future stepping of the product.
Fixed:	This erratum has been previously fixed.
NoFix:	There are no plans to fix this erratum.
(No mark) or (Blank Box):	This erratum is fixed in listed stepping or specification change does not apply to listed stepping.
Shaded:	This item is either new or modified from the previous version of the document.

Number	B0	Plans	ERRATA
E1	X	NoFix	tVAL(min) Timing Is Not Meeting AGP 3.0 Specification
E2	X	NoFix	AGP Prefetch Cache Must Be Disabled

Number	SPECIFICATION CHANGES
	There are no Specification Changes in this Specification Update revision.

Number	SPECIFICATION CLARIFICATIONS
	There are no Specification Clarifications in this Specification Update revision.

Number	DOCUMENTATION CHANGES
	There are no Documentation Changes in this Specification Update revision.

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Errata

1.	**tVAL(min) Timing Is Not Meeting AGP 3.0 Specification**
Problem:	During simulation studies, it was determined that the AGP signals were not meeting the tVAL(min) of 1ns.
Implication:	AGP interface is susceptible to latching invalid data.
Workaround:	Minimum trace lengths for the AGP common clock and source synchronous signals have increased to offset this timing violation. Refer to latest platform design guide.
Status:	No fix planned for this erratum. Issue resolved by board workaround.
2.	**AGP Prefetch Cache Must Be Disabled**
Problem:	System hangs can occur during AGP transactions when the AGP Prefetcher is enabled.
Implication:	System hang.
Workaround:	Disable AGP Prefetch Cache by clearing bit 0 of AGP Miscellaneous Register (Device 1 Function 0 Offset A0-A3h).
Status:	No fix planned for this erratum. System performance is not affected by this erratum.

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Specification Changes

There are no Specification Changes in this Specification Update revision.

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Specification Clarifications

There are no specification clarifications in this Specification Update revision.

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Documentation Changes

There are no Documentation Changes in this Specification Update revision.