



Intel[®] 7500 Scalable Memory Buffer

Specification Update

March 2010

Notice: The Intel[®] 7500 Scalable Memory Buffer may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are available on request.

Reference Number: 323167-001



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Contents

Revision History	4
Preface	5
Summary Tables of Change	7
Identification Information	10
Errata	11
Specification Clarification	16
Specification Changes	17
Documentation Changes	18



Revision History

Revision Number	Description	Date
001	• Initial release of the document.	March 2010



Preface

This document is an update to the specifications contained in the Affected Documents table below. This document is a compilation of device and documentation sightings, specification clarifications and changes. It is intended for hardware system manufacturers and software developers of applications, operating systems, or tools.

Information types defined in Nomenclature are consolidated into the specification update and are no longer published in other documents.

This document may also contain information that was not previously published.

Affected Documents

Document Title	Document Location
<i>Intel® 7500 Scalable Memory Buffer Datasheet</i>	Intel.com

Related Documents

Document Title	Location
JESD79-3 DDR3 SDRAM Specification	JEDEC

Nomenclature

Errata are design defects or errors. These may cause Intel® 7500 Scalable Memory Buffer behavior to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all sightings documented for that stepping are present on all devices.

Specification Changes are modifications to the current published specifications. These changes will be incorporated in any new release of the specification.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in any new release of the specification.

Documentation Changes include typos, errors, or omissions from the current published specifications. These will be incorporated in any new release of the specification.

S-Spec Number is a five-digit code used to identify products. Products are differentiated by their unique characteristics, for example, core speed, L2 cache size, package type, etc. as described in the processor identification table. Read all notes associated with each S-Spec number.

ODF Number is a four digit code used to distinguish between engineering samples. These samples are used for early qualification and early design validation. The functionality of these parts can range from mechanical only to fully functional.



Note: Errata remain in the specification update throughout the product's lifecycle, or until a particular stepping is no longer commercially available. Under these circumstances, sightings removed from the sightings report are archived and available upon request. Specification changes, specification clarifications and documentation changes are removed from the specification update when the appropriate changes are made to the appropriate product specification or user documentation (datasheets, manuals, and so forth).



Summary Tables of Change

The following tables indicate the sighting, specification changes, specification clarifications, or documentation changes which apply to the Intel 7500 Scalable Memory Buffer product. Intel may fix some of the sightings in a future stepping of the component, and account for the other outstanding issues through documentation or specification changes as noted. These tables use the following notations:

Codes Used in Summary Tables

Stepping

X:	A sighting exists in the stepping indicated. Specification Change or Clarification that applies to this stepping.
(No mark) or (Blank box):	This sighting is fixed in listed stepping or specification change does not apply to the listed stepping.

Platform

X:	A X, in the Intel® Itanium® Processor 9300 Series platform indicates the Intel 7500 Scalable Memory Buffer sighting exists in the Intel® Itanium® Processor 9300 Series platform. A X, in the Intel® Xeon® Processor 7500 Series (Boxboro-EX) platform indicates the Intel 7500 Scalable Memory Buffer sighting exists in the Intel® Xeon® Processor 7500 Series (Boxboro-EX) platform.
(Blank box):	This sighting does not apply to the platform.

Page

(Page):	Page location of item in this document.
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Status

Doc:	Document change or update will be implemented.
Plan Fix:	This sighting may be fixed in a future stepping of the product. Plan Fix (HW) indicates that the fix will be implemented in silicon.
Fixed:	This sighting has been previously fixed.
No Fix:	There are no plans to fix this sighting.

Row

	Change bar on outside margins indicates this sighting is either new or new or modified from the previous version of the document.
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Intel 7500 Scalable Memory Buffer Sightings Summary

Number	Platform		Status	Sightings
	Intel® Itanium® Processor 9300 Series Platform	Intel® Xeon® Processor 7500 Series Platform		
1	X	X	No Fix	During a hard reset CKE may remain active for a short period of time after clocks have stopped.
2	X	X	No Fix	Voltage Offset Cancellation (VOC) issue can affect SMI training reliability.
3	X	X	No Fix	Intel® SMI link fails to train with TS1 errors being reported.
4	X	X	No Fix	Incorrect status information being logged into the SBCALSTATUS CSR.
5	X	X	No Fix	JTAG access to unimplemented CSR causes busy bit to be stuck at '1'.
6	X	X	No fix	MEMBIST based CMD2DATA training value is 1 clock lower than is usable with the host initiated Intel® SMI transactions.
7	X	X	No Fix	Physical Damage To Intel SMI Lane Can Cause Training To Fail. Lane and clock failover will not be supported.
8	X	X	No fix	Enabling Membist Power Save bit can cause a delay in the time it takes for self refresh entry on a fast reset sequence and may result in refresh time (trefi) violation.
9	X	X	No fix	CKE pins erroneously asserted when non-broadcast command is issued. This issue is not applicable to Intel host controller based designs.
10	X	X	No fix	The tSTAB timing requirement on the RDIMM Register may be violated when Intel 7500 Scalable Memory Buffer comes out of a fast reset sequence and DISSREXIT is cleared.
11	X	X	No fix	MemBIST: Usage of Dynamic Address Inversion (DAI) feature with non user defined data pattern and start/end address range results in data miscompares.
12	X	X	No fix	Overshoot/Undershoot specification for DDR clock may be violated when Intel 7500 Scalable Memory Buffer is powered down.
13	X	X	No fix	After a resync reset, a SMBus read to certain specific Intel 7500 Scalable Memory Buffer CSRs may result in incorrect data being returned by Intel 7500 Scalable Memory Buffer.
14		X	No fix	Intel 7500 Scalable Memory Buffer may not drive the disable_b code during pC3E events.
15	X	X	No fix	Upon entry into disable_a state as a result of loss of forward clock; Intel 7500 Scalable Memory Buffer may falsely detect a failover forwarded clock and cause Intel SMI training to fail.

Specification Changes Summary

No.	Documentation Changes



Specification Clarifications Summary

No.	Documentation Changes
1	

Documentation Changes Summary

No.	Documentation Changes



Identification Information

Component Identification via Programming Interface

The Intel 7500 Scalable Memory Buffer stepping can be identified by the following register contents:

Vendor ID	Device ID	Revision Number
8086h	0380h	20h

Component Marking Information

The Intel 7500 Scalable Memory Buffer stepping can be identified by the following component markings:

QDF/S-Spec Number	Top Marking	Notes
SLH2F	BD7500MB	



Errata

1. During a hard reset CKE may remain active for a short period of time after clocks have stopped.

Problem: During a hard reset CKE may remain active for a short period of time after clocks have stopped.

Implication: This is a violation of the DDR specification. Since DIMMs will be reset, this is not expected to be an issue.

Workaround: None at this time.

Status: For the steppings affected, see the Summary Table of Changes.

2. Voltage Offset Cancellation (VOC) issue can affect Intel SMI training reliability.

Problem: The default trim range for VOC is insufficient in some cases when canceling p-n offsets, thus compromising SMI training reliability.

Implication: SMI will not train.

Workaround: For Intel® Itanium® processor 9300 series platforms a SAL fix has been implemented in Intel® QuickPath Interconnect/SAL/Memory Reference Code (MRC), revision 0.67. For Intel® Xeon® Processor 7500 Series Platform use the Reference Code (RC) V0.63. In RC 0.65 the w/a is included in Fbd2Init.c line#2919 routine FBD_STATUS InitAmbPreFbdTraining() Line#3124-3127

```
AmbReg &= ~(BIT20+BIT21+BIT22);
```

```
AmbReg = AmbReg | (BIT22 | BIT21);
```

```
if ((Status = WriteAmbSmb(Host, &(*ChAmbList)[Amb], AMB_FBDRXPICTRL,
AmbReg)) !=
```

```
FBD_SUCCESS)
```

Status: For the steppings affected, see the Summary Table of Changes.

3. Intel SMI link fails to train with TS1 errors being reported.

Problem: Intel SMI link fails to train with TS1 errors being reported.

Implication: Link initialization failures will prevent the system from booting.

Workaround: Set bit (device 0, function 7, offset F8h, bit 1) to a '1'. A SAL fix has been implemented in the next revision of the Intel QuickPath Interconnect/SAL/Memory Reference Code (MRC), V0.68a. For Intel® Xeon® processor 7500 series platform use the Reference Code (RC) V0.71.

1	RWS	0	Setting This bit allows additional 2UI for frame_clk to core_clk setup time
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The workaround is in Fbd2Init.c routine InitFbdClocks()

Line#1941-1945

```
// Increase 2UI for frame_clk to core_clk setup time
if ((Status = ReadAmbSmb(Host, &(*ChAmbList)[0], AMB_SBDEFEATURE,
&AmbReg)) != FBD_SUCCESS)
    return Status;
```



```
        if ((Status = WriteAmbSmb(Host, &(*ChAmbList)[0],  
AMB_SBDEFEATURE, AmbReg | BIT1 | BIT10)) != FBD_SUCCESS) return  
Status;
```

Status: For the steppings affected, see the Summary Table of Changes.

4. Incorrect status information being logged into the SBCALSTATUS CSR.

Problem: Incorrect status information is being logged in the SBCALSTATUS CSR, device 0, function 1, offset 7Ch.

Implication: SBCALSTATUS may record an incorrect failure, even though the Intel SMI link is training successfully.

Workaround: The Intel® Xeon® Processor 7500 Series platform reference code will check P_CSR_PBOXFS2.InitDone (D:0x18 F:2 Offset:0x84 Bit[4]) in the host to ensure initialization has completed successfully.

Status: For the steppings affected, see the Summary Table of Changes.

5. JTAG access to unimplemented CSR causes busy bit to be stuck at '1'.

Problem: JTAG access to unimplemented CSR causes busy bit in JTAG chain to be stuck at '1'.

Implication: JTAG cannot be used to access unimplemented CSRs.

Workaround: Avoid reading unimplemented CSRs using JTAG interface.

Status: For the steppings affected, see the Summary Table of Changes.

6. MEMBIST based CMD2DATA training value is 1 clock lower than is usable with the host initiated Intel SMI transactions.

Problem: When using MEMBIST to train the cmd2data value, membist is able to pass with a cmd2data value that is 1 clock lower than what is usable with host initiated Intel SMI transactions.

Implication: Incorrect CMD2DATA setting may result in data corruption case being observed by host.

Workaround: The workaround is for BIOS to add 1 clock to the value computed by MEMBIST based CMD2DATA training. For Intel Itanium processor 9300 series platforms, a future version of the Intel® QuickPath Interconnect/SAL/Memory Reference Code (MRC) is expected to contain a workaround. For Intel® Xeon® Processor 7500 Series platforms use reference code V0.72.

```
//Membist is 1 clock off from actual cmd2data value so add an extra clock. HSD Intel  
7500 Scalable Memory Buffer Sighting [3349188]: CoarseDelay += 1;
```

Status: For the steppings affected, see the Summary Table of Changes.

7. Physical Damage To Intel SMI Lane Can Cause Training To Fail.

Problem: Noise on an Intel SMI lane can appear as a TS0 training header to the Intel 7500 Scalable Memory Buffer receiver causing training to fail. This is seen on Intel SMI lanes which have some physical damage (generally connector, trace, or pad connectivity issues). For this issue to occur there must be physical damage to the lane to cause reflection, and the noise at the receiver needs to match the TS0 header during Intel SMI training.

Implication: A retraining can be caused by memory initialization, RAS event, or firmware generated fast reset. Anytime one of these events occurs and a lane with physical damage is present, this condition can occur. When this condition occurs, the Intel SMI link will attempt to retrain (up to the retry threshold) to recover. If the number of retrains exceeds the retry threshold, a fatal Error# 608\610 (Zbox Uncorrectable Memory Link CRC Error) will occur which will cause a fatal MCA.



Workaround: In the Intel host Memory Controller, set PZ[n]_PBOXFCTL1.RETRY_THR to '0111 to enable multiple retraining attempts. With this value, achieving the retry threshold due to this issues is expected to be a very rare event. In a rare case the retry threshold is met, this will cause the Intel SMI link to fail with a fatal error. The damage to the lane will log an Error# 617 or 618 (Zbox Correctable Memory Link CRC Error, Northbound or Southbound with lane mapout) on the processor. A future PAL release will change the PAL Reset Value for this CSR field to '0111. Firmware can also set this CSR as described.

Status: No Fix.

8. **Enabling Membist Power Save bit can cause a delay in the time it takes for self refresh entry on a fast reset sequence, resulting in refresh time (trefi) violation.**

Problem: Enabling power save bit (function 2, offset 40h, bit 20) can cause a delay in the time it takes for self refresh entry on a fast reset sequence, resulting in a trefi (7.8 us) timing violation.

Implication: A time delay greater than 7.8 μ s constitutes a refresh timing violation and may subsequently result in dram memory failures.

Workaround: When enabling power save bit, set RSTREQERR (function 3, offset 6Ch, bit 7:0) to a value of 08h. This will reduce the time taken to go into self refresh on a fast reset sequence and prevent the trefi violation.

Status: For the steppings affected, see the Summary Table of Changes.

9. **CKE pins erroneously asserted when non-broadcast command is issued.**

Problem: There are 3 slots (A-B-C) per SMI frame. The following commands can be in any of the slots as long as they're not causing any collision on DDR control signals.

SRE (Self Refresh Entry/Exit)

PDE (Power Down Entry/Exit)

CKE per DIMM

CKE per RANK

The commands can be used to control individual CKE or all CKE's of the same DDR channel. If TWO of the above commands happen to be in the same SMI frame (occupying any 2 slots of the frame) and are targeting CKE's on different channels (this is allowed since there's no collision on CKE pins); it could cause incorrect CKE being asserted to both channels. The issue does not exist if the above commands are in different SMI frames. This issue was found as a result of pre-silicon validation. This issue has not been observed in post-silicon as Nehalem-EX processor, Westmere-EX processor, Intel Itanium processor 9300 series, Poulson processor hosts are not capable of issuing 2 of these transactions in the same frame.

Implication: Erroneous CKE pin assertion may subsequently result in unpredictable system behavior.

Workaround: None at this time. This issue does not occur on IA platforms, as Intel hosts do not issue 2 of these commands in the same frame.

Status: For the steppings affected, see the Summary Table of Changes.

10. **The tSTAB timing requirement on the RDIMM Register may be violated when Intel 7500 Scalable Memory Buffer comes out of a fast reset sequence and DISSREXIT is cleared.**

Problem: tSTAB is a period of 6us required by the register on the RDIMM where clocks must be stable before CKE is pulled high. Intel 7500 Scalable Memory Buffer begins driving DDR clocks in TS0 and CKE can be pulled high by the host in the LO state or by Intel 7500



Scalable Memory Buffer in the TSO state (when DISSREXIT: function 3, offset 74h, bit 16, is cleared). The Intel SMI Architecture and Protocol specification mentions that DRAM clocks must be stable before entering the testing state, but the register requires 6 us in addition to the stable clock needed by the DRAMs. If the DISSREXIT is cleared then the CKE's will be pulled high in TSO and this may violate the tSTAB timing.

Implication: tSTAB timing violation may result in ECC/UECC errors.

Workaround: Ensure DISSREXIT functionality in Intel 7500 Scalable Memory Buffer is not used/cleared. The Intel 7500 Scalable Memory Buffer DISSREXIT CSR cannot be used to pull CKEs high after a training event. The host will be required to pull the CKEs high. The host will need to ensure 6us has expired between TSO state and the time the CKEs are pulled high. This can be achieved by driving a longer TS1 pattern.

Status: For the steppings affected, see the Summary Table of Changes.

11. MemBIST: Usage of Dynamic Address Inversion (DAI) feature with non user defined data pattern and start/end address range results in data miscompares.

Problem: The DAI feature only works with user defined data pattern and user defined start/end address. Usage of DAI with other data types and address patterns will result in data miscompares. Also in DAI mode, the least significant address bit will be fixed at a '0' or '1' depending on the programmed starting address, that is, LSB of address field does not invert.

Implication: DAI usage model is restricted to user defined data pattern and start/end address.

Workaround: Use DAI feature only with user defined data pattern and user defined start/end address range; ATYPE = 10 and DTYPE = 01.

Status: For the steppings affected, see the Summary Table of Changes.

12. Overshoot/Undershoot specification for DDR clock may be violated when Intel 7500 Scalable Memory Buffer is powered down.

Problem: When a system is powered down the Overshoot/Undershoot specification for the DDR clock signal as defined by the "max OS/US area" in the JEDEC "DDR3 DRAM VDD AC OS/US" specification may be violated. Values of 0.30 V-ns to 0.35 V-ns have been observed against a spec requirement for the maximum allowed area of 0.19 V-ns.

Implication: No functional issues have been observed or expected as a result of this issue. Register vendors have confirmed that violation of this specification will not result in any issues.

Workaround: None at this time.

Status: For the steppings affected, see the Summary Table of Changes.

13. After a resync reset, a SMBus read to certain specific Intel 7500 Scalable Memory Buffer CSRs may result in incorrect data being returned by Intel 7500 Scalable Memory Buffer.

Problem: After a resync reset, SMBus read to certain Intel 7500 Scalable Memory Buffer CSRs result in zeros being returned to the requestor. The CSRs include fdbnbcfg0nxt, fdbnbcfg1nxt, fdbnbcfg0cur, fdbnbcfg1cur, stuckl, nbfibpgctl, nbfibtxen, nbfibtxshft, nbfibtsct, nbfibinit, nbibistmisc, nbfibpattbuf1 and nbfibportctl.

Implication: Incorrect read return data may result in a system hang

Workaround: After writing to linkfrqnx, wait 300 us and toggle BIT 1 of function 7, offset C4h.

Status: For the steppings affected, see the Summary Table of Changes.

14. Intel 7500 Scalable Memory Buffer may not drive the disable_b code correctly during pC3E events.

Problem: Intel 7500 Scalable Memory Buffer may not drive the disable_b code correctly during pC3E events, resulting in a SMI training hang, unless Intel 7500 Scalable Memory



Buffer is reset i.e. RST_N pin asserted. pC3E is a power saving feature during which the host may turn off the forwarded clocks to Intel 7500 Scalable Memory Buffer upto several times per second. The issue has been observed on the BXB-EX platform with pC3E feature enabled. This may also happen during system warm-reset, that do not reset Intel 7500 Scalable Memory Buffer before allowing Intel SMI accesses.

Implication: System may hang as result of Intel 7500 Scalable Memory Buffer not driving the disable_b code northbound.

Workaround: Disable pC3E feature in the host.

Status: For the steppings affected, see the Summary Table of Changes.

15. Upon entry into disable_a state as a result of loss of forward clock; Intel 7500 Scalable Memory Buffer may falsely detect a failover forwarded clock and cause Intel SMI training to fail.

Problem: Upon entry into disable_a state as a result of loss of forwarded clock; Intel 7500 Scalable Memory Buffer may falsely detect a clock on the failover clock lane for a short time, and cause the Intel SMI training to fail. The failure occurs because Intel 7500 Scalable Memory Buffer does not drive the disable state code northbound. The host reports a disable state code failure. Setting the host CSR PZ[n]_PBOXFCTL1.RETRY_THR to '0111 to enable multiple retraining attempts does not resolve the issue. This issue is more likely to occur with the pC3E feature enabled on Intel® Xeon® Processor 7500 Series platform. pC3E is a power saving feature during which the host turns off the forwarded clock to Intel 7500 Scalable Memory Buffer. This issue has been observed with pC3E testing on the Intel® Xeon® Processor 7500 Series platform during which the host may turn off the forwarded clock to Intel 7500 Scalable Memory Buffer several times per second. During this high rate of forwarded clock loss with pC3E active there is a significant probability for failure. Without pC3E induced forwarded clock loss events, the probability of normal clk failover exposing this issue is expected to be very low. Sighting analysis shows that clock lane failover due to physical clock lane damage is exposed the same as in sighting 62, and clock lane failover will provide incrementally improved functionality in the presence of physical clock lane damage.

Implication: System may hang as a result of Intel 7500 Scalable Memory Buffer not driving the disable state code back to the host.

Workaround: If pC3E feature is enabled, forwarded clock failover can only be supported at time T= 0 (initial boot). Disabling the failover clock detection feature at runtime would make Intel 7500 Scalable Memory Buffer stay on the clock that was detected during initial SMI link training. If pC3E feature is disabled, only a physical damage on the clock lane can result in loss of forwarded clock to Intel 7500 Scalable Memory Buffer. When pC3E is disabled, it is recommended to keep the forwarded clock failover mechanism enabled.

Status: For the steppings affected, see the Summary Table of Changes.



Specification Clarification

There are no new Specification Clarification in this Specification Update revision.



Specification Changes

There are no new Specification Changes in this Specification Update revision.



Documentation Changes

There are no new Documentation Changes in this Specification Update revision.

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